ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-4761

Design Guide for Protection of Printed Board Via Structures

IPC-4761
July 2006 A standard developed by IPC

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1219
Tel. 847.615.7100 Fax 847.615.7105
www.ipc.org

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.

Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.

IPC-4761

Design Guide for Protection of Printed Board Via Structures

Developed by the Via Protection Task Group (D-33d)
of the Rigid Printed Board Committee (D-30) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Via Protection Task Group (D-33d) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Rigid Printed Board Committee

Chair
Susan Hott
Robisan Laboratory

Via Protection Task Group

Chair
Susan Hott
Robisan Laboratory

C. Don Dupriest
Lockheed Martin Missiles and Fire Control

Technical Liaisons of the IPC Board of Directors

Peter Bigelow
IMI Inc.

Sammy Yi
Flextronics International

Via Protection Task Group

David R. Backen, TTM Technologies

Scott A. Bowles, Hallmark Circuits Inc.

Mark Buechner, BAE Systems

Dennis J. Cantwell, Printed Circuits Inc.

Rick Carlson, Taiyo America Inc.

Denise Chevalier, Amphenol TCS

Thomas Clifford, Lockheed Martin Space Systems Company

Christopher Conklin, Lockheed Martin Corporation

David J. Corbett, Defense Supply Center Columbus

Werner Engelmaier, Engelmaier Associates, L.C.

Alan Exley, Cosmotronic

Thomas G. Farrell, Underwriters Labs Inc.

Dennis Fritz, MacDermid, Inc.

Lionel Fullwood, WKK Distribution Ltd.

Mahendra S. Gandhi, Northrop Grumman

Michael R. Green, Lockheed Martin Space Systems Company

Michael E. Hill, Colonial Circuits Inc.

Thomas E. Kemp, Rockwell Collins

Dana W. Korf, Sanmina-SCI Corporation

Steve Larson, Amphenol TCS

Gary B. Long, Intel Corporation

Michael G. Luke, C.I.D., Raytheon Company

James F. Maguire, Intel Corporation

Chris Mahanna, Robisan Laboratory Inc.

Kenneth J. Manning, Raytheon Company

Brian C. McCrory, Delsen Testing Laboratories

Susan Morgana, United Technologies

Peter A. Navarro, BAE Systems

Diana Niesser, Huntsman Advanced Materials

Benny Nilsson, Ericsson AB

Stephen G. Pierce, SGP Ventures, Inc.

Randy R. Reed, Merix Corporation

Karl A. Sauter, Sun Microsystems Inc.

Joseph C. Schmidt, Raytheon Missile Systems

Bob Sheldon, Pioneer Circuits Inc.

Gordon Sullivan, Huntsman Advanced Materials

Dung Q. Tiet, Lockheed Martin Space Systems Company

David A. Vaughan, Taiyo America, Inc.

Vicka White, Honeywell Inc.

Dewey Whittaker, Honeywell Inc.

Michael W. Yuen, Foxconn EMS, Inc.

Table of Contents

Figures

Tables

Design Guide for Protection of Printed Board Via Structures

1 SCOPE

The protection of through vias within Printed Wiring Boards (PWB) has evolved from limited use to common practice. Technology has evolved where via fabrication techniques and protection methodologies need to be defined to allow current designs to be manufacturable at an acceptable yield and cost. Numerous techniques and objectives exist, and will be discussed in this document. This document is the product of the IPC D-33d Via Protection Task Group and has been developed to provide guidance for the designer and fabricator on how via protection should be approached as well as guidance on how via protection should be specified in procurement documentation.

1.1 Purpose This guideline provides PWB designers, fabricators and/or users with information on existing methods for the protection of vias on printed boards. In addition to detailing some of the advantages of via protection, production and material issues are given to aid the user in evaluating the benefits and concerns for each type of protection.

1.2 Terms and Definitions The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

Bumped Via Protection – Via protection where the hole plugging or fill material protrudes above the surface of the hole interface producing a convex shape. See Figure 1-1.

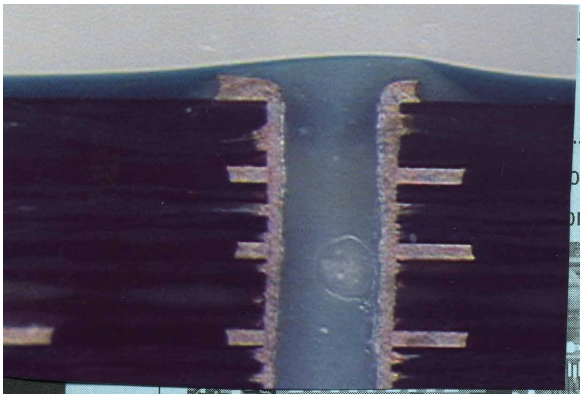


Figure 1-1 Bumped Via Protection Material

Dimpled Via Protection – Via protection where the hole plugging or fill material recedes below the hole interface producing a concave shape. See Figure 1-2.

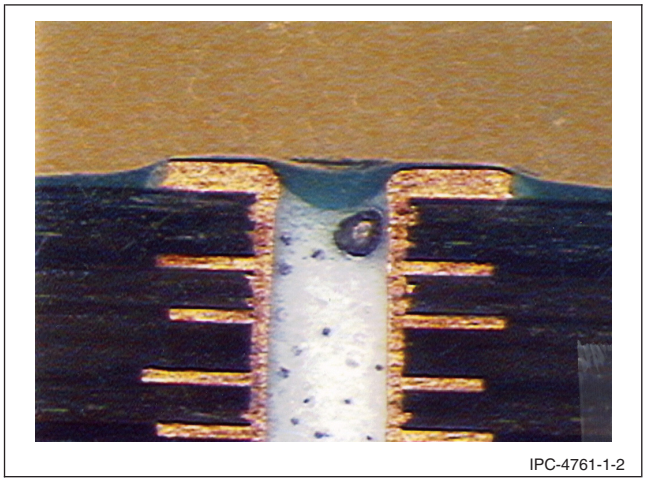


Figure 1-2 Dimpled Via Protection Material

Planarized Via Protection – Via protection where the excess hole plugging or fill material protruding above the hole interface has been removed by a process to produce a coplanar surface. See Figure 1-3.

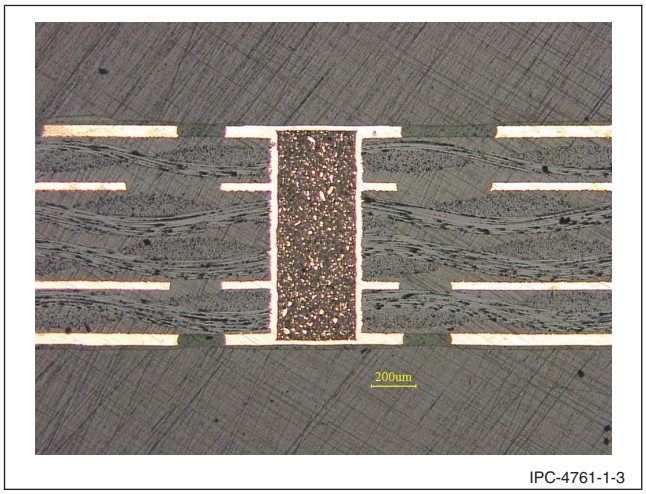


Figure 1-3 Planarized and Capped Via Protection Material

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-A-600 Acceptability of Printed Boards

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

[1]www.ipc.org

IPC-2221 Generic Standard on Printed Board Design

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

3 PWB FABRICATION AND ASSEMBLY GUIDELINES

Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.

There are a number of advantages with providing protection for interconnect vias; however, there are just as many production issues within the PWB fabrication and assembly processes that users must consider.

3.1 Advantages of Via Protection Some of the advantages of protecting vias include the following, though not every advantage is applicable for every via protection type described in 5.1 through 5.7:

- Prevent corrosion caused by PWB fabrication processes such as plating or flux residue, from either fabrication or assembly, from passing through or becoming trapped in plated-through holes (PTHs).
- Improve vacuum handling, placement of surface mount technology (SMT) parts by sealing the surface and to prevent air leakage during In Circuit Test (ICT). Unfilled through hole via holes may contribute to intermittent test probe contact as a result of probe contamination when air is pulled through the unfilled via.
- Prevent solder ball blowout during assembly processes, i.e., wave or reflow, that utilize solder paste
- Prevent solder mask creep into holes
- Reduces solder paste loss
- Isolate via holes of conventional PWB products within the assembly soldering process to prevent migration, shorts, and contamination entrapment under components
- Fill/Flush Vias within build-up cores to ensure planarity for subsequent dielectric layer formation and dielectric separation, or to assure adequate resin fill in the subsequent bonding process
- Prevent migration of adhesives and encapsulants used during assembly under rigid area array integrated circuit (IC) packaging substrates.
- Prevent flux from flowing through vias which can inhibit the curing of bonding adhesives.

For specific advantages of each protection type, see Table 5-1.

3.2 PWB Fabrication Issues There are a number of issues in the PWB fabrication process that need to be taken into consideration when evaluating a protection methodology, including the following:

- Partial plugging can result in solder from the Hot Air Solder Level (HASL) operation being trapped within the vias. During subsequent reflow soldering the solder can be expelled by trapped gasses forming large solder balls on the surface.
- Application of final finishes following single-sided techniques can result in circumferential voids within the surface finish in vias being tented or plugged and may result in reliability issues such as corrosion of exposed copper.
- Adhesion of tent or plug material to final finishes.
- Plugging of vias from both sides of the hole results in manufacturability and reliability issues.
- Process methods and/or manufacturing complexity may vary depending upon the requirements of the end-customer application.
- Hole fill or plug with either solder mask or epoxy fill compound can be difficult to perform depending upon the process used. Voids within high modulus fill or plug materials can be a significant concern, particularly when those voids are in direct contact with the PTH wall, causing a long-term reliability stress riser. Check with specific fill material manufacturer to determine if modulus data is available. Voids located near the surface SMT contact pad are also cause for concern. For these reasons, voids should be kept to a minimum.
- The Coefficient Thermal Expansion (CTE) mismatch characteristic is known to sometimes cause barrel cracks within the hole wall.
- Use of partial via plugging should only be done after application of inert final surface finishes to avoid potential chemical attack to the via hole wall. Partial plugging or tenting from one side can result in bare copper in the via. See 3.4 for additional information on chemical entrapment in plugged vias.
- Application of HASL final finish prior to partial via plugging requires a unique plug operation. HASL imparts a melting metal coating to the copper via wall which is very different from non-melting metal applications; there is consequently no adhesion of the plug material to the barrel of the via, so the plug must be anchored to the laminate and/or solder mask surface surrounding the via for it to stay in place during soldering.
- Utilization of a final finish that does not contain inert metals, such as organic solderability preservative (OSP) coatings, can be a concern for protecting hole wall copper from corrosion. When using OSP finishes it is recommended to use a complete fill operation (see 5.5) or a two-sided tent and cover application (see 5.2).

- Liquid Photo-Imageable (LPI) solder mask is often used to plug vias. However, any solvent containing ink which is forced into a via hole will have difficulty drying the plug of ink in the hole and residual solvents can ″pop″ later during soldering operations. Also, LPI inks rely on UV and/or thermal energy for their cure, making it difficult to get sufficient UV light down through the plug to get good cure. There are however LPI fill materials on the market that have been specifically optimized for UV cure and, in such cases, high aspect ratio vias are a non-issue for curing.
- Electroless nickel immersion gold (ENIG) plating offers variation in plugged via structures. The plugging operation can be performed before or after metallization. One instance utilizes an LPI dot pattern to open the vias, followed by ENIG metallization and then plugging from one side (see 5.3). Another instance utilizes metallization first followed by a plug operation with a subsequent LPI covering (see 5.4). The resulting difference in appearance among the two techniques is the opening in the LPI that is required to allow the plating into the hole.

3.2.1 Fill or Plug Separation from Plated Hole Wall There exists the potential for separation of the fill or plug material from the knee of the plated hole which may entrap chemistry as shown in Figure 3-1. When establishing a protection methodology it is recommended that a maximum allowable depth be established for both hole fill separation and dimples, as shown in Figure 3-1 and 3-2.

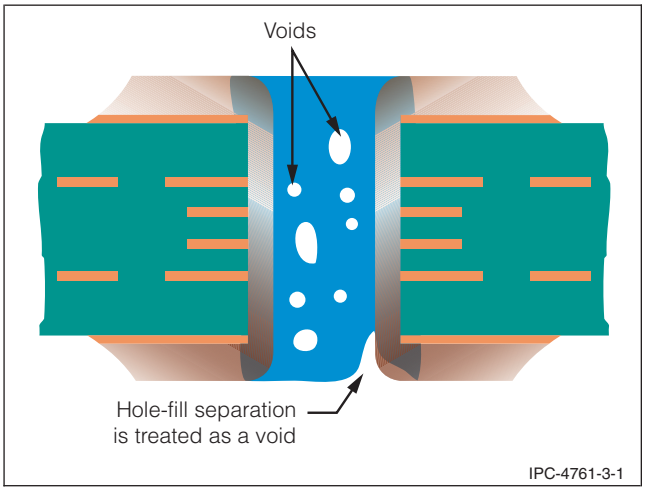


Figure 3-1 Example of Hole Fill/Plug Separation from Plated Hole Wall

3.2.2 Voids Voids can be a concern where material is used to provide a partial plug or complete fill of a via. See Figure 3-3 and Figure 3-4 for examples of voids in via fill material.

3.3 Assembly Process Issues There are several issues in the assembly process that are unique:

- The use of a solder paste stencil requires contact with a flat surface topography to provide a gasketing effect around the solder pad openings.

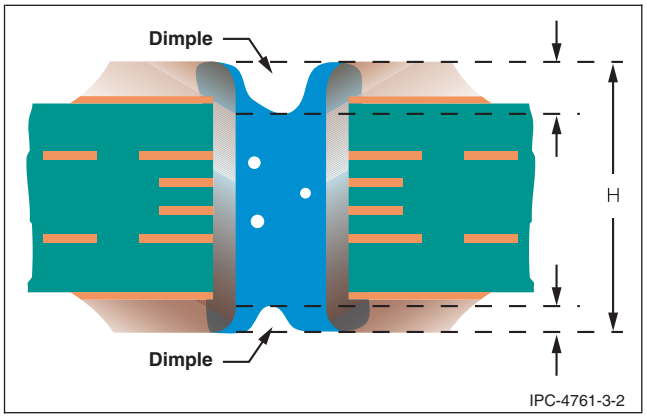


Figure 3-2 Example of Dimples Within Fill/Plug Material

Figure 3-3 Voids in Via Fill Material

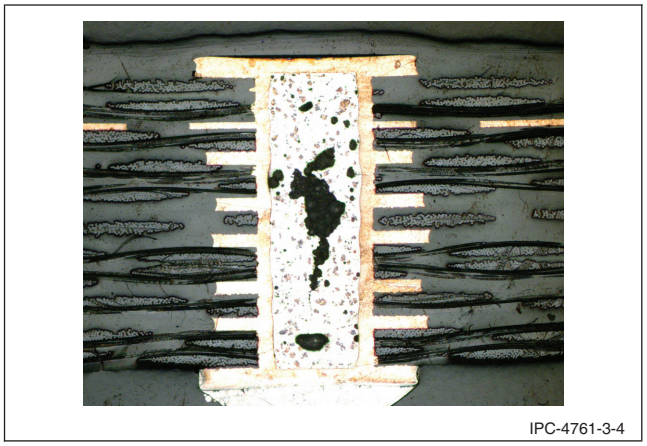


Figure 3-4 Large Voids in Via Fill Material

- Bump height, which is defined as the difference between the height of the mask over the via and the height of the adjacent solderable land, can affect or interrupt the solder stencil paste application. It has been commonly noted in industry that a bump height of 0.076 mm [0.003 in] or greater can cause a non-contact effect on the application of solder paste.
- Vias can serve as a reservoir to entrap flux or other contaminates that become difficult or impossible to clean. This is all especially true when they lie under the component outline.

- Vias can act as a thermal path to draw away solder volume from the solder joint.
- Via cracking at solder reflow temperatures.
- Entrapped air, when heated, will expand and crack the solder mask tent or cover material. This allows the solder mask tent over the vias to expand upward creating coplanarity issues. During this air expansion the pushing of the tent upwards can result in a crack due to this pressure. This cracking can create an opening and trap solutions within what has become a semi-sealed via.

3.4 Long-Term Reliability Concerns Single-sided via protection (Types I-a, II-a and III-a) should not be used with bare copper hole walls. Any attempt to apply a surface finish to a hole wall that is not protected by the plug material resulting from a partial penetration into the via will result in a bare copper area at the plug material/hole barrel interface. This bare copper area will be attacked by any chemicals entrapped within the hole during board fabrication, as well as those trapped during assembly processes (the partial plug process may have gaps between the plug material and the hole wall allowing entrapment of chemicals). The resulting contamination can combine with moisture and corrode the thickness of the hole wall plating to a degree where the plating is no longer able to withstand the stresses of operating temperatures common in assembly processes as shown in Figure 3-5. Final finishes should be applied prior to plugging.

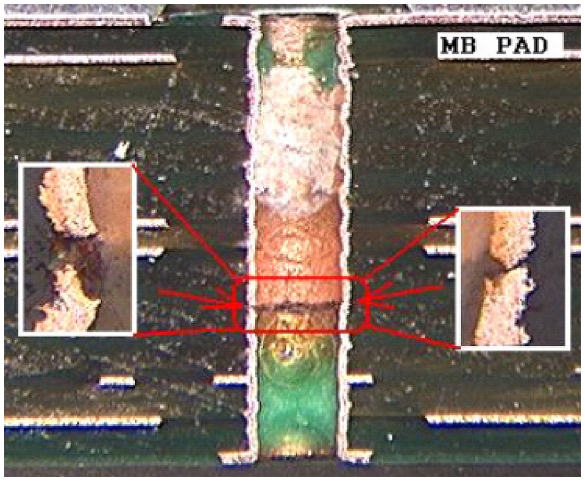


Figure 3-5 Corroding of Hole Wall Plating Resulting from Single-Side Via Protection

4 MATERIALS/DESIGN CONSIDERATIONS

Materials currently being used to protect vias include standard liquid photoimageable and non-imageable solder masks, dry film solder masks, specially formulated hole plugging inks, conductive inks, liquid dielectric materials and even materials not used in other PWB constructions.

When selecting or approving materials to protect vias in PWBs there are a number of performance criteria for the material that should be considered based upon how the PWBs are designed and used. For example, the material could be totally encapsulated inside a multilayer structure in an innerlayer, or exposed to the outside environment, or something in between. The end use will determine the specific material characteristics needed for the application.

The key questions deal with the use of the material in the PWB construction, and the reason(s) why the vias must be protected or plugged. Some typical reasons for protecting vias are to:

- Prevent solder and chemistry from migrating to the opposite side of the board in assembly
- Prevent contamination from migrating into bare copper surface finish holes/vias
- Assure good vacuum in bed-of-nails electrical testing
- Prevent solder wicking into vias, causing insufficient solder joints
- Increase circuit density – when the protected vias are very close to component mounting pads
- Recover real estate – as in via-in-pad where the material must be plated over
- Prevent resin starvation or voids in sub-composite vias in multi-layer lamination
- Provide electrical or thermal conductivity

Those specifying protected vias need to understand the importance of the cost/benefit relationship. Protection of vias often requires the use of specially developed materials. The plugging process can require additional investment in equipment and/or be labor-intensive, both of which are cost adders. Because of the wide range of materials and equipment employed for via filling, one should expect a significant variation in finished quality and ease of inspection.

4.1 End Use Considerations The operating environment of the finished assembly will dictate the performance parameters that the hole filling material must withstand. Some examples are:

- Humidity – PWBs that will be exposed to high humidity should pass hydrolytic stability testing
- Maximum operating temperature – CTE and Glass Transition Temperature (Tg) may be important for high temperature applications
- Temperature cycling and thermal shock – If the PWB must pass this testing, the plugging material must also be tested with the board. Test coupons on panels should have all via protection styles used on the board represented.
- Non-nutrient testing - Applies to the plugging material if exposed to the environment

- Outgassing – A particular concern if the material is inside a multilayer or plated over, or in space applications

From a design perspective, some features that have an effect upon the material selection and degree of difficulty for filling are:

- Diameter of vias – Very small holes can take longer to fill or plug; very large holes may be difficult as well
- Aspect ratio – High aspect ratio holes are more difficult to fill or plug
- Circuit Density (The proximity of exposed pads to protected vias) – A photoimageable plugging material may be needed to prevent contamination that would cause assembly defects
- Electrical Testing Requirements – The desire to have a partially filled via such that a pad on one side may be used as a test point may dictate the PWB construction (surface finish) and plugging material selection

4.2 Fabrication Considerations The PWB fabricator will often have several different materials that can be selected to protect vias. The choice is generally the material that:

1) Is already specified, approved or qualified in the facility and/or by the Electronics Manufacturing Services (EMS) customer
2) Gives the minimum cost and highest yield in production
3) Provides the least disruption to process flow
4) Is compatible with existing equipment and processes in the shop including:
   - Application with minimal voids
   - Curing (Thermal or UV)
   - Planarization Plating (if required)
5) Is already listed in the fabricator's UL Flammability file

4.3 Assembly Considerations The material used to plug the vias must survive all of the conditions and chemistries that will be seen by the PWBs in assembly without failure. Although the plug material does not typically need the electrical performance of a solder mask, it will need to have certain physical, thermal and chemical properties. Some of the issues for selecting a via protection material are:

1) Assembly temperatures and chemistries – The material must be capable of withstanding typical process conditions that will be seen by the PWB.
2) Planarity requirements – This includes:
   - Height restrictions to prevent assembly defects
   - Amount of shrinkage during processing to avoid non-planarity (dimples) in the final plug
   - If plated, the adhesion of the plating to the plug to avoid "doming" of the plating
3) Flux and cleaner compatibility
4) Conformal coating compatibility
5) Substrate compatibility

4.4 Types of Materials for Filled/Plugged Via holes are typically filled by either screen printing, direct squeegee or with a pressurized applicator. The ease of filling depends upon the via diameter and aspect ratio, viscosity of the plugging material, particle size of filler particles, and the filling equipment and process parameters.

4.4.1 Non-conductive (Organic) – Non-imageable Non-conductive, non-imageable materials are polymeric and may be filled with materials that increase viscosity and inhibit shrinkage during processing and curing. They are usually cured with thermal and/or UV energy. They can be used in most any application except where enhanced thermal or electrical conductivity is needed. Some of these materials are not easily plated, so, if plating over the material is needed, it is important to verify platability with the supplier and fabricator.

4.4.2 Non-conductive – Photoimageable Photoimageable materials are characterized by their ability to be used in very high circuit density areas such as Ball Grid Array (BGA) patterns without danger from bleeding or smearing of the plugging material onto component mounting pads that will inhibit soldering. Any material outside the imaged area will be developed off, leaving all component pads clean.

4.4.3 Conductive Ink Conductive hole plugging materials are polymer-based and filled with metal particles, usually silver or copper. The post-cure thermal and electrical characteristics depend upon the properties of the chosen polymer and metal composition. High metal loading of these materials tends to reduce the shrinkage induced by curing. It may also improve the ease of plating since the metal is conductive and autocatalytic (and may not require swell and etch or electroless plating).

4.5 Materials for Tented/Covered Via Structures

4.5.1 Tented Only Tenting involves the use of dry film solder mask (liquid solder mask will not tent holes). For tenting applications that will not be covered with a liquid solder mask, a thicker dry film (greater than or equal to 0.076 mm [0.003 in]) should be used to provide the needed integrity to the tent.

4.5.2 Tented and Covered With this application a thinner dry film solder mask (less than or equal to 0.058 mm [0.0023 in]) may be considered to keep overall thickness of mask over the annular ring of the via below the maximum allowed. The thickness of the liquid mask that covers the tent may also need to be minimized to help keep overall thickness within specification.

4.6 Material Specification and Selection In many cases it is important for the via plug or fill material, or the desired properties of the material, to be specified. The following is a list of parameters to be considered:

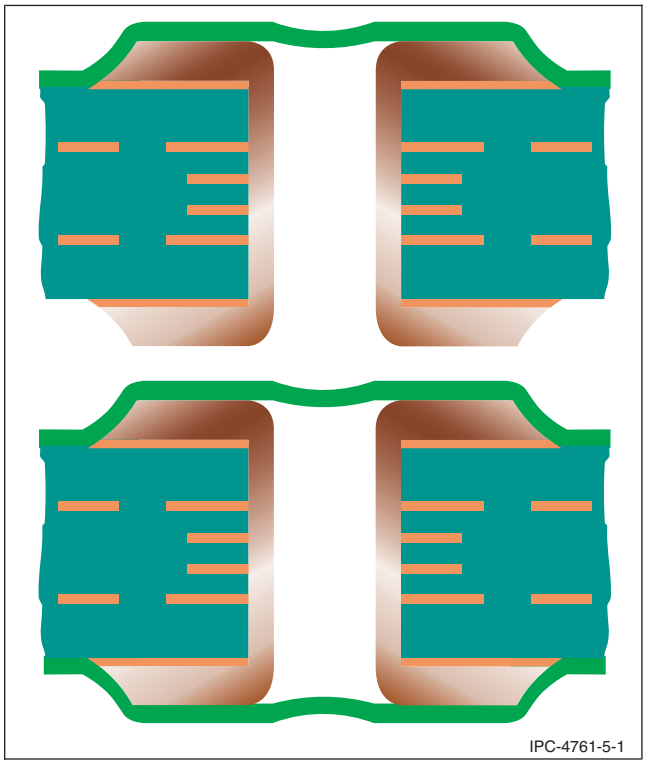
1) For all applications:
   - Flammability – Materials must be UL approved if the PWB is UL certified
   - Plating – When required, capable of being plated uniformly
   - Plating adhesion - Minimize separation from the fill material during subsequent processing when required.
   - Fill or Plug Adhesion – When required, materials must not separate from any metallized surface
   - Voids – Degree of voiding within via fill material
2) When Fully Encapsulated (by plating or inside a multilayer structure):
   - CTE
   - Tg
   - Outgassing
3) When Exposed to the Environment (not fully encapsulated)
   - Hydrolytic Stability
   - Non-nutrient
   - Compatibility with other processes or materials including:
     a) Assembly flux
     b) Assembly post cleaning chemistry
     c) Conformal coating (adhesion issue)
4) For plating applications:
   - Ease of planarization before plating
   - Shrinkage during processing/curing (dimple issue)
   - Ability to roughen, catalyze and plate easily (organic fill materials)
5) PWB Density Issues:
   - Material may need to be photo-imageable if intended for application over fine pitch surface features.
6) Special Requirements:
   - Thermal Conductivity
   - Electrical Conductivity
   - NASA Outgassing
   - Color for Final Inspection

5 VIA PROTECTION DEFINITIONS AND TYPES

The types of via protection currently identified by the IPC D-33d IPC Via Protection Task Group are depicted in this section. It should be noted that Figure 5-1 through Figure 5-8 do not illustrate all of the surface possibilities, including dimples, bumps or planarized surfaces in the mask material, that are commonly found over the hole. See Table 5-1 for a listing of application guidelines identifying those protection types best suited for a given process. Descriptions of specific via protection types can be found in 5.1 through 5.7.

The PWB designer may specify requirements or degree of planarity depending on end-item needs and manufacturing capability.

5.1 Tented Via (Type I Via) A via with a dry film mask material applied bridging over the via wherein no additional materials are in the hole (see Figure 5-1). It may be applied to one side (Type I-a) or both sides (Type I-b) of the via structure:



Single Sided Tented Not Recommended
Figure 5-1 Examples of Type I Tented Vias

Type I-a

Process: Vacuum laminated film material that is photodefinable.

Benefits: A consistent and repeatable process providing excellent hole tenting and uniform thickness.

Concerns: Protection should not be used with bare copper hole walls (see 3.4). Chemical entrapment. Requires specialized application equipment and handling regarding cleanliness to meet Surface Insulation Resistance (SIR) requirements and damage. Unsupported films have the potential for puncture. Inert final finishes should be applied prior to tenting to prevent entrapment. Tents are not recommended over melting metal finishes; however, if applied then the tent

Table 5-1 Application Guidelines for Via Protection Types[1]

Description (Type)	Applications									
	Before Final Finish	After Non-Melting Metal Final Finish	Prevent air leakage in ICT (Vacuum Seal)[2]	Keeping chemistry or solder from passing through the via	Keeping chemistry or solder from being trapped in the via	Dielectric protection of via land	Fill holes in cores prior to lamination	Improves surface planarity	Best For thermal conductivity[3]	Prevent migration of solder, adhesives or encapsulants into vias
Tented - Single-Sided (Ia)	NOT RECOMMENDED[5]									
Tented - Double-Sided (Ib)	X	X	X	X	X	X				X
Tented and Covered – Single-Sided (IIa)	NOT RECOMMENDED[5]									
Tented and Covered – Double-Sided (IIb)	X	X	X	X	X	X				X
Plugged – Single-Sided (IIIa)	NOT RECOMMENDED[5]									
Plugged - Double-Sided (IIIb)	X	X	X	X	X	X		X		X
Plugged and Covered – Single-Sided (IVa)	NOT RECOMMENDED[5]									
Plugged and Covered Double-sided (IVb)	X	X	X	X	X	X				X
Filled (fully plugged) (V)	X	X	X	X	X		X	X	X	X
Filled and Covered (VI)	X	X	X	X	X	X				X
Filled and Capped (VII)[4]	X	X	X	X	X		X	X	X	X

1) Descriptions of specific types of via protection are provided in 5.1 through 5.7.
2) Not recommended over melting metals.
3) It is recommended to use a thermally conductive hole filling ink (e.g. silver ink).
4) When specifying Via-in-Pad, it is recommended that Type VII via protection be used.
5) See 3.4 for concerns associated with single sided via protection.

should extend beyond the pad to cover laminate material in order to prevent lifting of the tent material during subsequent soldering operations. Dimples may be a concern for adhesive processes where a glue dot is used for component placement.

Type I-b

Process: Vacuum laminated film material that is photo-definable.

Benefits: A consistent and repeatable process providing excellent hole-tenting and uniform thickness. This process typically results in a clean hole.

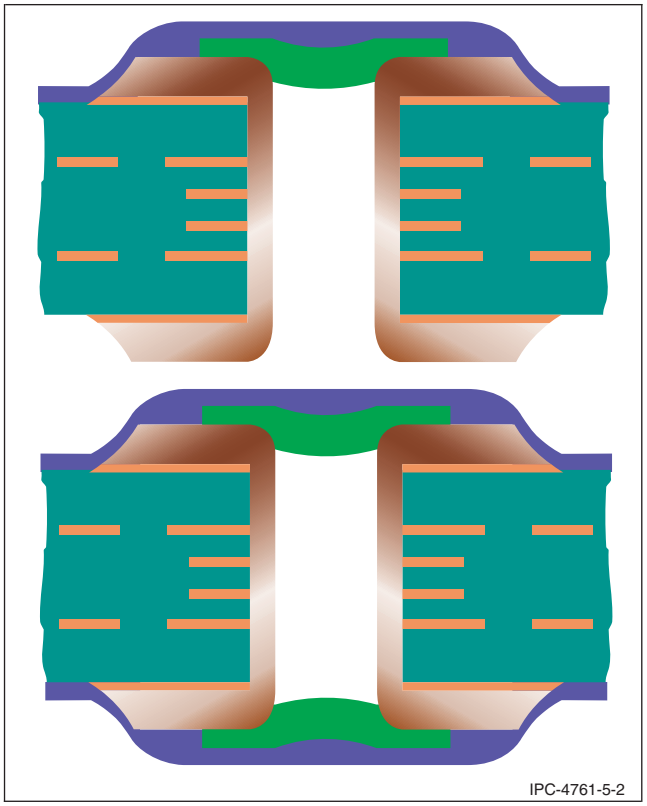
Concerns: Requires specialized application equipment and handling regarding cleanliness to meet SIR requirements and damage. Unsupported films have the potential for puncture. Dimples may be a concern for adhesive processes where a glue dot is used for component placement.

5.2 Tented and Covered Via (Type II Via) A Type I via with a secondary covering of mask material applied over the tented via (see Figure 5-2). The material may be applied to one side (Type II-a) or both sides (Type II-b) of the via structure:

Type II-a

Process: Application of mask over Type I.

Benefits: Improved tenting strength over Type I.



Single Sided Tented and Covered Not Recommended
Figure 5-2 Examples of Type II Tented and Covered Vias

Concerns: Increased processing and height of multiple coatings. Dimples may be a concern for the adhesive process where a glue dot is used for component placement. Chemical entrapment. Inert final finishes should be applied prior to tenting to prevent entrapment. Tents are not recommended over melting metal finishes; however, if applied then the tent should extend beyond the pad to cover laminate material in order to prevent lifting of the tent material during subsequent soldering operations.

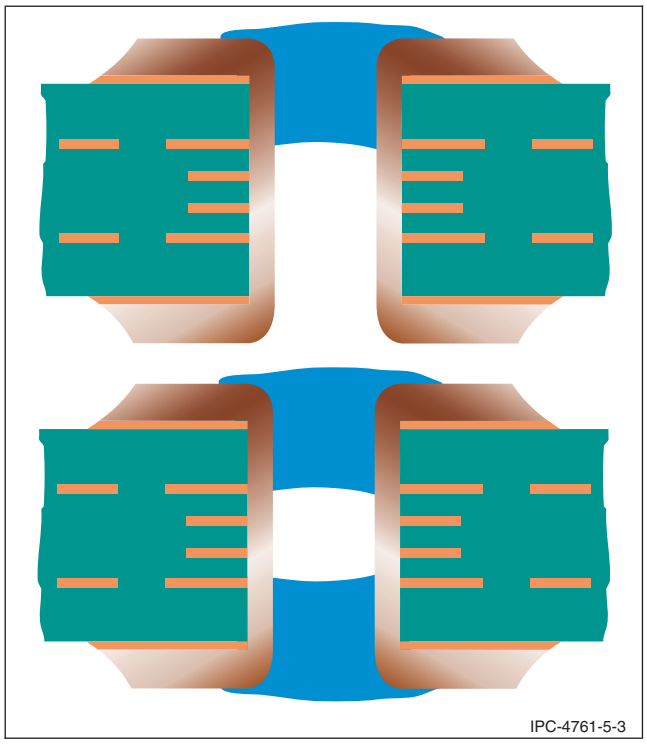
Type II-b

Process: Application of mask over Type I.

Benefits: Improved tenting strength over Type I.

Concerns: Increased Processing and height of multiple coatings. Dimples may be a concern for the adhesive process where a glue dot is used for component placement. Usage of standard dry film mask material will result in significant bump height. Bumps may be a concern in lifting the solder paste stencil. A conforming mask material is recommended to prevent significant increases in bump height.

5.3 Plugged Via (Type III Via) A via with material applied allowing partial penetration into the via (see Figure 5-3). The plug material may be applied from either one side (Type III-a) or both sides (Type III-b) of the via structure.



Single Sided Plugged Not Recommended
Figure 5-3 Examples of Type III Plugged Vias

Type III-a

Process: Screened and Roller Coated.

Benefits: Ease of processing. There are few manufacturing constraints.

Concerns: Protection should not be used with bare copper hole walls (see 3.4). The plug material may protrude out one side of the via. Outgassing.

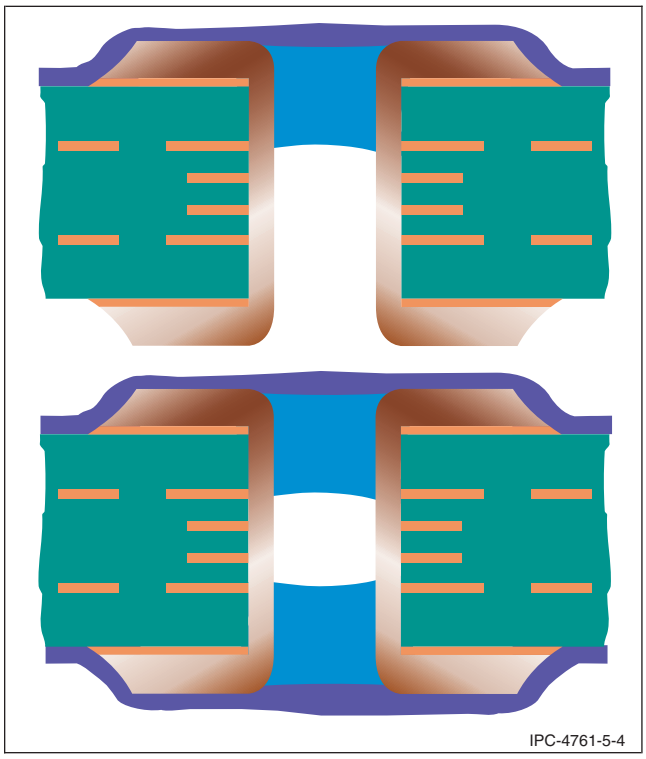
Type III-b

Process: Screened and Roller Coated.

Benefits: Ease of processing. There are few manufacturing constraints.

Concerns: Thermally induced volumetric expansion of entrapped contaminants or air for Type III-b. Air expansion or even entrapped solvents can have a significant effect on plugs as they are being cured, causing ″blow-out″. Process is difficult to produce consistently with thermally cured materials and LPI. Aspect ratio is a concern for the open part of a hole so that there can be sufficient removal of chemistries. See application guidelines in Table 5-1 for final finish applications.

5.4 Plugged and Covered Via (Type IV Via) A Type III via with a secondary covering of material applied over the via (see Figure 5-4). The plug and secondary covering material may be applied from either one side (Type IV-a) or both sides (Type IV-b) of the via structure.



Single Sided Plugged and Covered Not Recommended
Figure 5-4 Examples of Type IV Plugged and Covered Vias

Type IV-a

Process: Application of mask over Type III.

Benefits: Increased plug strength. Pin holes that occur through the use of Type III plugging can be mitigated through the use of this type.

Concerns: Protection should not be used with bare copper hole walls (see 3.4). Final finishes should be applied prior to plugging.

Type IV-b

Process: Application of mask over Type III.

Benefits: Increased plug strength. Pin holes that occur through the use of Type III plugging can be mitigated through the use of this type.

Concerns: Thermally induced volumetric expansion of entrapped contaminants or air for Type IV-b. Air expansion or entrapped solvents can have a significant effect on plugs as they are being cured, causing ″blow-out″. Process is difficult to produce consistently with thermally cured materials and LPI.

5.5 Filled Via (Type V Via) A via with material applied into the via targeting a full penetration and encapsulation of the hole (see Figure 5-5).

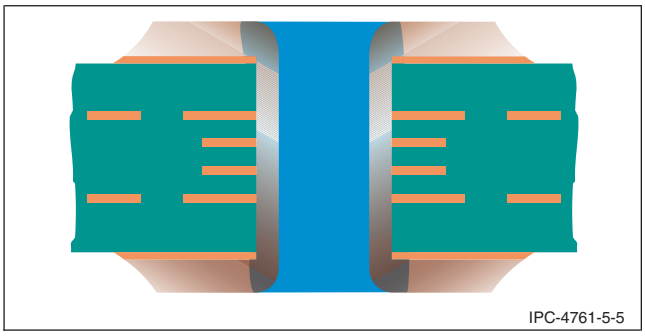


Figure 5-5 Example of Type V Filled Via

Process: Screened, roller-coated, or squeegeed.

Benefits: Complete fill of conductive or non-conductive material which eliminates contaminants. Process prevents solder balling. Benefits useful in sequential lamination processes.

Concerns: Voiding. The removal of excess material from the surface. Surface planarity. Complete curing. Excess process variables. Complexity of obtaining complete fill. CTE mismatch between the fill material and substrate.

5.6 Filled and Covered Via (Type VI Via) A Type V via with a secondary covering of material (liquid or dry film soldermask) applied over the via (see Figure 5-6 and Figure 5-7). The covering material may be applied from either one side (Type VI-a) or both sides (Type VI-b) of the via structure:

Process: Application of mask over Type V. Fill material can be electrically and/or thermally conductive depending on end use.

Benefits: Protection of the pad over Type V. The effects of surface voids possibly caused by using Type V method can be minimized with Type VI.

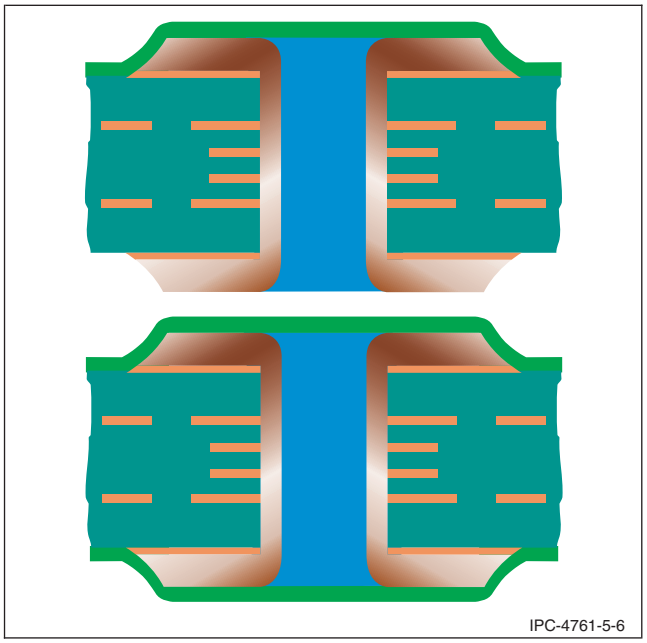


Figure 5-6 Examples of Type VI Filled and Covered Vias, Dry Film Cover

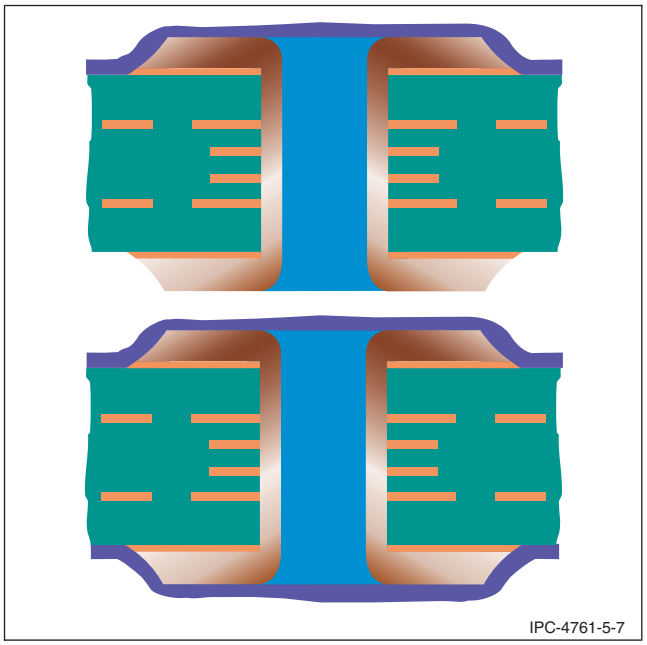


Figure 5-7 Examples of Type VI Filled and Covered Vias, Liquid Film Cover

Concerns: Same as Type V with additional processing.

5.7 Filled and Capped Via (Type VII Via) A Type V via with a secondary metallized coating covering the via (see Figure 5-8). The metallization is on both sides:

Process: Metallized coating over Type V. Applicable where high density features are required.

Benefits: Via-In-Pad and Ball-on-Via pad. Via stacking. Applicable where high density features are required. Benefits useful in sequential lamination processes.

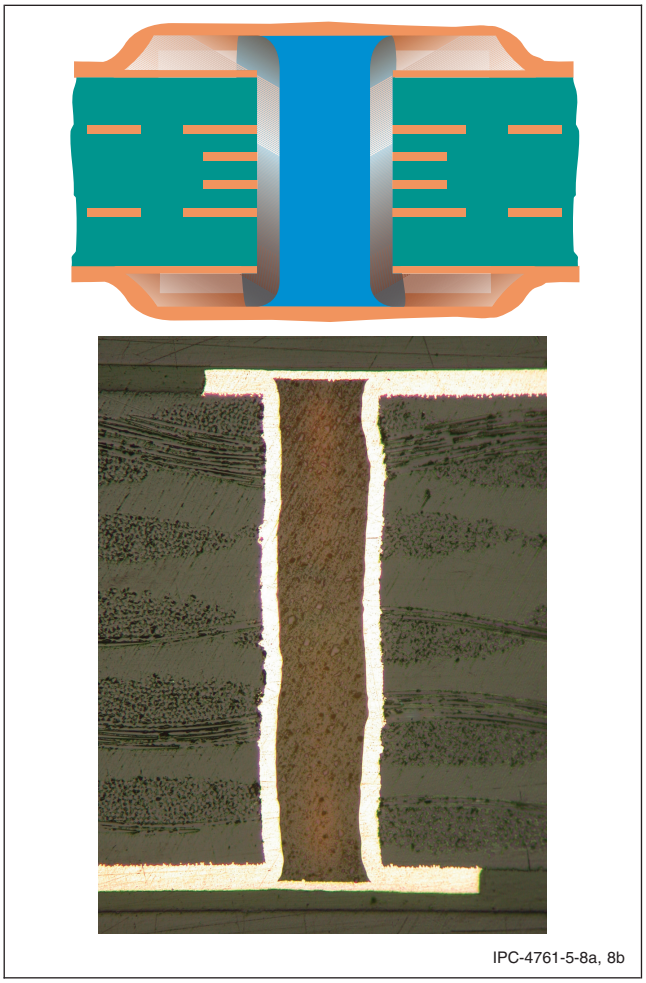


Figure 5-8 Examples of Type VII Filled and Capped Via

Concerns: Adhesion of the metallized coating to the via fill and copper pad. Copper thickness. The planarity between the fill material and the copper surface. CTE mismatch between the fill material and metallization resulting in air gap (fill material shrinkage). Less than 100% via fill may result in a metallized cap that is too thin or a dimple that can also cause entrapped air resulting in voids in BGA solder joints. Pinholes in the metallized coatings result in non-solderable areas of a land where the capped via is intended for a BGA solder joint. Reduced solder volume is also a concern with dimples.

5.8 Partially Filled Via Though not identified as a via protection type, this document does recognize manufacturing processes where solder mask flows into the hole during liquid solder mask application, without intending to provide complete coverage or protection, and may result in partial plugging (see Figure 5-9). This is not acceptable with bare copper surface finishes (see 3.4). The illustrations below show typical via configurations when liquid solder mask is used with no specific process for via protection. Inconsistency of coverage can lead to a mix of all configurations on the same board. Process should not be implemented over bare copper. If the final finish is HASL the center of the hole wall will be bare copper.

6 PERFORMANCE TRADEOFFS

There are a number of tradeoffs or concerns that the PWB designer and manufacturer should consider when evaluating a method of via protection.

6.1 Planarity In assembly it is typically important to have a relatively planar surface to the PWB as it is received from the PWB fabricator. In many cases components will be placed directly over protected vias and, if there is any bulge or bump at the via, the component will not sit firmly onto its mounting pad(s) creating the potential for a soldering defect(s). Dimples can cause entrapped air resulting in voids in BGA solder joints.

It is also very important to maintain this planarity through assembly soldering. Bulged, erupted or popped vias can dislocate components and cause soldering defects as above.

6.2 Via Metallization When vias are to be solder coated, before they are coated the plug of material in the hole can become loose as the solder reflows or melts during soldering processes. This can lead to either plug failure or a soldering defect. However, if this type of plug does fail, the copper of the hole wall is protected from chemical attack by the solder coating. Even though this practice may be more prone to failure, the consequences, in terms of long-term reliability, may not be as much of a concern.

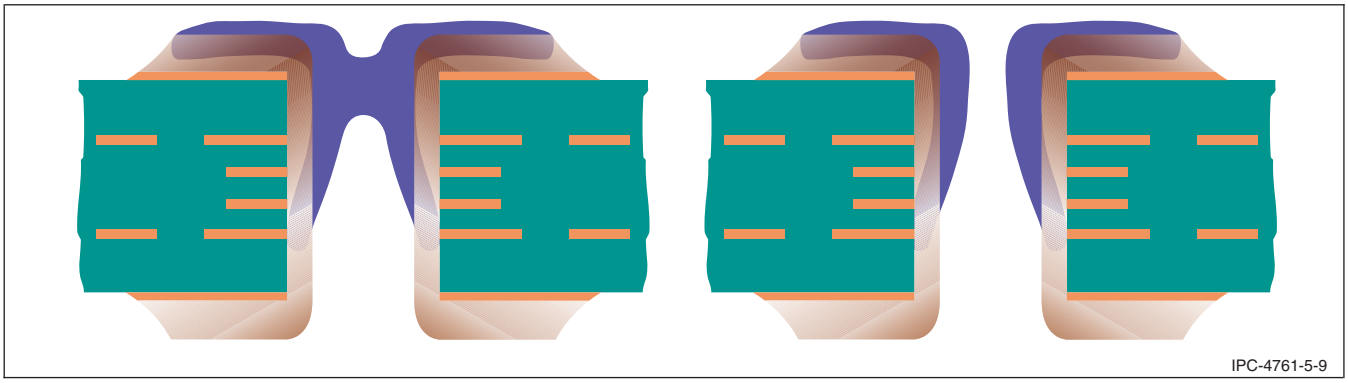


Figure 5-9 Examples of Partially Filled Vias

Bare copper protected vias are more likely to survive assembly processing because the plugging material can maintain excellent adhesion to the copper surface, just the same as to circuitry (assuming that an approved solder mask material is used). However, if a failure did occur, there could be a long-term reliability concern in that it could expose bare copper to chemistry and the environment. If the circuitry was gold plated, however, there would essentially be no concern from failed via protection because of the inertness of the gold.

6.3 Moisture Absorption Because materials used to plug vias can absorb moisture during storage, it may be necessary to bake PWBs with protected vias before soldering to eliminate absorbed moisture from the holes. This should increase the reliability of the via protection material through the soldering process.

6.4 Cleanliness Concerns If the plug is loosened the potential for flux and other contaminates being trapped between the loosened plug and hole wall is great. These contaminates can cause problems with surface resistivity performance if the PWB is to be used in an environment where there is moisture. Single-sided tents pose a similar concern for the entrapment of chemistries.

6.5 Use of Conformal Coating If the final use of the assembled board is in an environment with greater than 80% relative humidity, conformal coating should be used to slow down any moisture absorption. Use of a conformal coating would be strongly recommended when only one side of a via is protected for any use environment as the presence would further protect the opposite side of the via.

7 SAMPLE DESIGNS

The following is a design example of a Type II-b tented and covered via structure within a Ball Grid Array (BGA) footprint design on a PWB.

Typical Materials for Tented and Covered:

- Dry Film thickness: 0.058 mm [0.0023 in] as applied; 0.046 mm [0.0018 in] as cured.
- LPI: thickness: 0.018 mm – 0.030 mm [0.0007 in – 0.0012 in] applied and cured.

Figure 7-1 illustrates the "Tented and Covered" technique as applied to a BGA footprint design. The solderable pad area of the BGA uses a solder mask clearance around the pad as opposed to a solder mask defined pad in which the solder mask overlaps the copper solderable area. The feed-through via represents a typical signal escape routing path (dog bone pattern) and is shown protected from additional soldering processes by the technique. A dry film dot is first applied over the via only, forming the "tented" feature. Next the entire surface is "covered" with LPI solder mask except at the solderable openings.

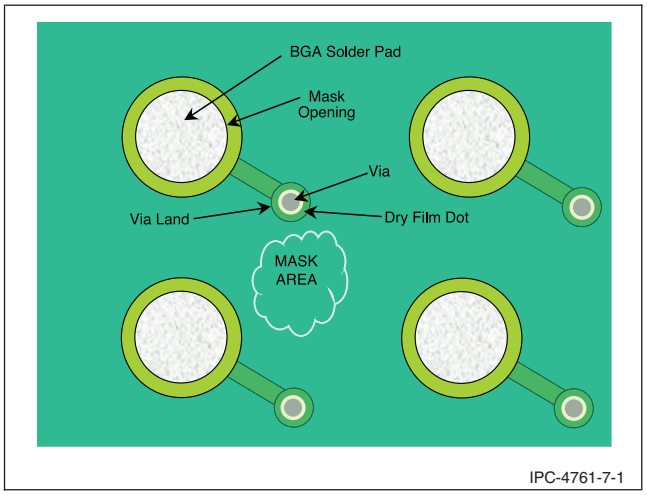


Figure 7-1 Illustration of "Tented and Covered" Via Protection Method

Figure 7-2 illustrates the variables used for calculating the feature sizes of the Type II-b Tented and Covered technique via a dimensioned cross-sectional view of both a PTH and a blind via feature. The design rule is provided in Figure 7-3.

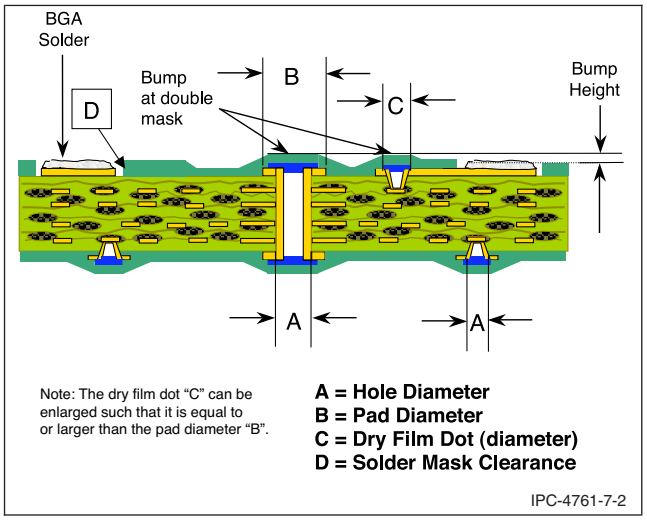


Figure 7-2 Cross-sectional View of Tent and Cover Detail

Figure 7-3 illustrates a single hole as a top view illustration to depict the solder mask clearance around a BGA solder pad.

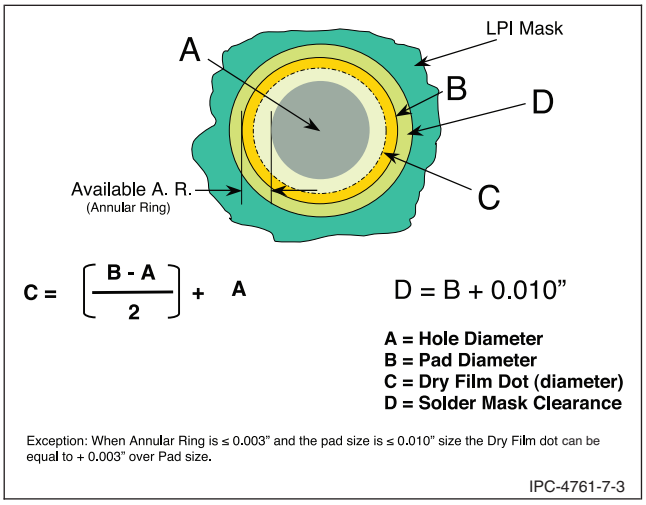


Figure 7-3 Top View Illustration of Solder Mask Clearance around a BGA Pad

Figure 7-4 illustrates a single hole as a top view illustration to depict the overlap detail of the tent and cover technique.

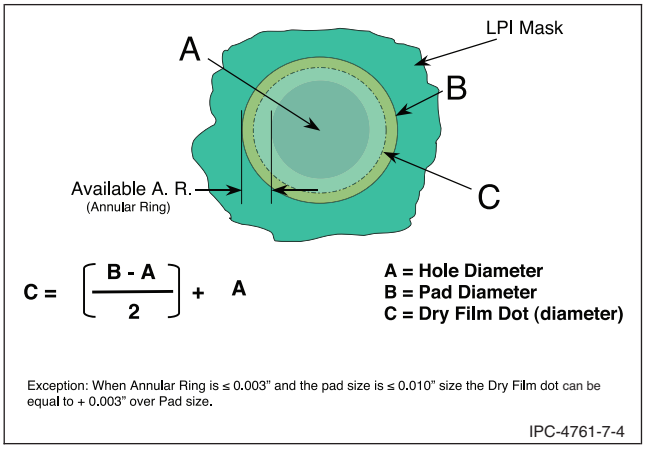


Figure 7-4 Top View Illustration of Overlap Detail for Tent and Covered Vias

The simplified formula also shown was developed to function as a design rule to quickly calculate the aperture sizes required to produce the artworks for a 2-step process. The noted exception was created as a safeguard to maintain feature sizes within the resolution capability of the solder mask materials. The basic goal of the applied rule is to produce a dot that splits the difference of the available annular ring.

8 EXAMPLES OF DRAWING NOTES

The following are examples of via protection call-outs, or notes, in printed board documentation:

Good procurement documentation will provide notation indicating how via protection is to be employed in the fabrication of the PWB to ensure that the user receives the desired product.

Note for Type V Vias
Indicated vias to be resin filled as described within 5.5 of IPC-4761 (Type V Filled Via). Selection of fill material shall be pre approved by user. Reduction of surface copper wrap due to via planarization shall not be greater than 50% of the specified minimum plated surface copper for that via structure.

Note for Type II-b Vias
All vias 0.305 mm [0.012 in] diameter or less shall be tented on both sides using a conforming dry film solder mask per IPC-SM-840, Class H prior to the application of LPI solder mask to create a Type II-b tented and covered structure (see 5.2 of IPC-4761). The dry film solder mask shall completely cover the via and shall not extend beyond the associated land. The combined height of the LPI solder mask and dry film solder mask shall not exceed 0.076 mm [0.003 in] above the covered pad surface. The height shall be verified by microsection evaluation of a representative quality conformance coupon.

IPC
ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1219
Fax: 847 615.7105

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: _____

Document(s) to which this term applies: _____

_____

_____

Committees affected by this term: _____

_____

_____

Office Use

IPC Office	**Committee 2-30**
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: _____	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: _____ Committee: IPC 2-30 Date: _____

This Page Intentionally Left Blank

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel: 847-615-7100 fax: 847-615-7105
www.ipc.org e-mail: answers@ipc.org

IPC World Wide Web Page www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignersCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, job opportunities and certification. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Trainingnews@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC Training Products.

leadfree.ipc.org

This forum acts as a peer interaction resource for staying on top of lead elimination activities worldwide and within IPC.

IPC_New_Releases@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC publications, updates and standards.

ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e.<mail list> @ipc.org), as it would be distributed to all the subscribers.

Example for subscribing:
To: LISTSERV@IPC.ORG
Subject:
Message: subscribe TechNet Joseph H. Smith

Example for signing off:
To: LISTSERV@IPC.ORG
Subject:
Message: signoff DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words, if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org. Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:
To: TechNet@IPC.ORG
Subject: <your subject>
Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori
tel: 847-597-2815 fax: 847-615-5615
e-mail: sasako@ipc.org www.ipc.org/emailforums

Education and Training

IPC conducts local educational workshops and national conferences to help you better understand conventional and emerging technologies. Members receive discounts on registration fees. Visit www.ipc.org to see what programs are coming to your area.

IPC Certification Programs

IPC provides world-class training and certification programs based on several widely-used IPC standards, including IPC-A-600, IPC-A-610, IPC/WHMA-A-620, J-STD-001 and IPC-7711A/7721A Rework and Repair. IPC-sponsored certification gives your company a competitive advantage and your workforce valuable recognition.

For more information on these programs:
tel: 847-597-2814 fax: 847-615-7105
e-mail: certification@ipc.org www.ipc.org/certification

Designer Certification (C.I.D.)/Advanced Designer Certification (C.I.D.+)

Contact:
tel: 847-597-2827 fax: 847-615-5627
e-mail: christipoulsen@ipc.org http://dc.ipc.org

EMS Program Manager Certification

Contact:
tel: 847-597-2884 fax: 847-615-5684
e-mail: susanfilz@ipc.org www.ipc.org/certification

IPC Video Tapes and CD-ROMs

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness. Members receive discounts on purchases.

For more information on IPC Video/CD Training, contact Mark Pritchard
tel: 505/758-7937 ext. 202 fax: 505/758-7938
e-mail: markp@ipcvideo.org http://training.ipc.org

IPC Printed Circuits Expo, APEX and the Designers Summit

This yearly event is the largest electronics interconnection event in North America. With technical paper presentations, educational courses, standards development meetings networking opportunities and designers certification, there's something for everyone in the industry. The premier technical conference draws experts from around the globe. 500 exhibitors and 6,000 attendees typically participate each year. You'll see the latest in technologies, products and services and hear about the trends that affect us all. Go to www.GoIPCShows.org or contact shows@ipc.org for more information.

Exhibitor information:

Mary Mac Kinnon
Director, Show Sales
847-597-2886
MaryMacKinnon@ip c.org

Alicia Balonek
Director, Trade Show Operations
847-597-2898
AliciaBalonek@ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Director
tel: 847-597-2809 fax: 847-597-7105
e-mail: JeanetteFerdman@ipc.org www.ipc.org

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Thank you for your decision to join IPC, Association Connecting Electronics Industries. IPC membership is site specific, which means that benefits of IPC membership are extended only to employees at the site that is designated on this application.

To help IPC serve your member site in the most effective manner possible, please tell us what work is being done at your site by choosing the most appropriate member category. *(Check one box only.)*

❑ INDEPENDENT PRINTED CIRCUIT BOARD MANUFACTURER

This facility manufactures, and sells to other companies, printed wiring boards (PWB's) or other electronic interconnection products on the merchant market.

What products do you make for sale?

❑ One- and two-sided rigid, multilayer printed boards ❑ Flexible printed boards ❑ Other interconnections

Site General Manager_____
Name Title

❑ EMSI COMPANY - Independent Electronics Assembly

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Site General Manager_____
Name Title

❑ OEM - Original Equipment Manufacturer

This facility purchases and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line?

_____

Site General Manager _____
Name Title

❑ INDUSTRY SUPPLIER

This facility supplies raw materials, machinery, equipment, or services used in the manufacture or assembly of electronic interconnection products.

What products or services does your company supply? (50 word limit, please)
The information that you provide here will appear in the next edition of the IPC Membership Directory.

Our company supplies:

_____

_____

_____

_____

❑ GOVERNMENT AGENCY/ACADEMIC TECHNICAL LIAISON

This government agency or accredited university, college or technical training school is directly concerned with design, research and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Please proceed to page 2 to complete the membership application.

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Site Information: (Please print or type)

Company Name

Street Address

City	State	Zip/Postal Code	Country

Main Switchboard Phone No	Main Fax No.

Company E-Mail Address	Website URL

Name of Primary Contact for all IPC matters	Title	Mail Stop

Phone No.	Fax No	E-Mail

Name of Senior Management Contact:	Title:	Mail Stop

Phone No	Fax No	E-Mail

Please attach business card of primary contact here.

Please designate your site's Technical Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

Please designate your site's Management Representatives:

For PWB/PWA design-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For PCB fabrication-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

For Electronics Assembly-related information and activities:

Contact Name	Title	Phone	Fax	E-mail

Please proceed to page 3 to complete the membership application.

Application for IPC Site Membership

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

MEMBERSHIP DUES SCHEDULE

Please check one:

- ❑ **$1,000.00 –** Annual dues for Primary Site Membership Twelve months of IPC membership begins from the time the application and payment are received at the IPC office.
- ❑ **$800.00 –** Annual dues for Additional Facility Membership
  An additional membership for a site within an organization where there already is a current Primary Site IPC membership.
- ❑ **$600.00** –** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. USD
  ** Please provide proof of annual sales.
- ❑ **$250.00 –** Annual dues for Government Agency or Academic Technical Liaison Membership. Must be not-for-profit organization.

TMRC MEMBERSHIP

- ❑ Please send information on participation in the Technology Market Research Council (TMRC) program. Only current IPC member sites are eligible to participate in this **calendar year** program, which is available for an additional fee.
- ❑ **Yes, sign up our site now:**
  $950.00 - Primary TMRC member site
  $400.00 - Additional facility TMRC member. Another site within our organization is already a TMRC program participant.

Name of Primary Contact for all TMRC matters:

_____

_____
Phone Fax

_____
E-Mail

PAYMENT INFORMATION

Enclosed is our check/money order for $_____

Mail application with check or money order to:

IPC
3491 Eagle Way
Chicago, IL 60678-1349

Fax or mail application with credit card payment to:

IPC
***3000 Lakeside Drive, Suite 309S**
Bannockburn, IL. 60015-1249
Tel: 847-615-7100
Fax: 847-615-7105
**** Overnight deliveries to this address only***

Please bill my credit card (circle one) for $_____

❑ MasterCard ❑ American Express ❑ Visa ❑ Diners Club

_____
Account No Expiration Date

_____
Name of Card Holder

_____
Authorized Signature

_____
Phone Number

QUESTIONS?

Call the IPC Member Services Department in Bannockburn, Illinois, at 847-597-2809 or 847-597-2872, or fax us at 847-615-7105.

E-mail: JeanetteFerdman@ipc.org SusanStorck@ipc.org

Please proceed to page 4 to complete the membership application.

Application for IPC Site Membership

INFORMATION DISTRIBUTION

IPC has significant member benefits available to a wide range of individuals within your organization. To ensure that your facility takes advantage of these benefits, please provide the name of the individual responsible for each of the functional areas listed below. If one person has multiple responsibilities, please list that person's name as many times as necessary.

Chief Executive:

Name | Title/Mail Stop | Phone | Fax | E-mail

Sales/Marketing:

Name | Title/Mail Stop | Phone | Fax | E-mail

Finance (CFO)

Name | Title/Mail Stop | Phone | Fax | E-mail

Human Resources

Name | Title/Mail Stop | Phone | Fax | E-mail

Environmental/Safety

Name | Title/Mail Stop | Phone | Fax | E-mail

Design/Artwork

Name | Title/Mail Stop | Phone | Fax | E-mail

Product Assurance

Name | Title/Mail Stop | Phone | Fax | E-mail

Manufacturing

Name | Title/Mail Stop | Phone | Fax | E-mail

Training

Name | Title/Mail Stop | Phone | Fax | E-mail

Purchasing

Name | Title/Mail Stop | Phone | Fax | E-mail

IPC REVIEW SUBSCRIPTION LIST

One of the many benefits of IPC membership is a subscription to the IPC *Review,* our monthly magazine. Please list below the names of individuals who would benefit from receiving our magazine, which provides information about the industry, IPC news, and other items of interest. A subscription for the IPC Primary Contact person is entered automatically.

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

Standard Improvement Form

IPC-4761

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1219
Fax 847 615.7105
E-mail: answers@ipc.org

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name Telephone

Company E-mail

Address

City/State/Zip Date

ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

ISBN #1-580987-70-2

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1219
Tel. 847.615.7100 Fax 847.615.7105
www.ipc.org